REMARKS

In view of the following remarks, Applicants respectfully request reconsideration and allowance of the subject application. This amendment is believed to be fully responsive to all issues raised in the February 26, 2004, Office action ("Office action").

Objections to the Drawings

The figures were objected to for the use of abbreviation "Fig." rather than "FIG." in the view numbers. Corrected drawings are submitted herewith on separate papers for approval by the Office.

Objections to the Claims

The objection to claim 7 stated: "Claim 7, because of its particular construction, is to be treated as an independent claim. Applicant must pay the necessary additional fees."

Claim 7 has been canceled.

General Discussion of Flash Technology and Cited References

When a request to read or write data is made to a flash memory device, the request typically indicates a logical addresses to which the data is to be written, not a physical address. As such, flash memory devices typically have some way to map the logical addresses received to a physical addresses in the flash memory

device. Typical flash memory devices use what is referred to as a logical-to-physical **block** mapping to perform this function.

In logical-to-physical **block** mapping, a logical-to-physical **block** map is used to locate a physical **block** in the flash memory that corresponds to a logical **block** address received in the write request. A sector offset or sector address included in the block address is then used to identify the particular sector where the data is to be written. Since the sector offset or sector address is identical in the logical and physical blocks, it is not necessary to use the sector offset or address when constructing or referring to the logical-to-physical **block** map.

In contrast to logical-to-physical **block** mapping, various implementations of the present application use logical-to-physical **sector** mapping. In logical-to-physical **sector** mapping, a logical-to-physical **sector** map is used to locate a physical **sector** in the flash memory that corresponds to a logical **sector** address received in the write request. That is, a logical-to-physical **sector** map includes an entry for each logical **sector** and a corresponding physical **sector**.

Both the Fujimoto et al. and Bruce et al. references use some form of logical-to-physical **block** map. Mitani includes a management table that "describes the correspondence between the physical and logical addresses." Mitani does not, however, specify the types of addresses that are used in the management table (e.g., block, sector, etc.). As such, neither Mitani, nor the other cited references, describe a logical-to-physical **sector** map.

The difference between logical-to-physical **sector** mapping and logical-to-physical **block** mapping is not trivial. Logical-to-physical **sector** mapping allows logically contiguous data sectors to be written to non-contiguous physical sectors in the flash. This ability is exploited in the systems and methods of the present application to provide, among other things, unique methods of data handling (reading/writing), defective sector management, and wear leveling.

CLAIM REJECTIONS

Claims Rejected Under - 35 USC §102(b)

Each of claims 1 – 44 has been rejected under 35 USC §102(b) as being anticipated by Bruce et al. (USPN 6,000,006). Additionally, each of claims 1 – 44 has been rejected under 35 USC §102(b) as being anticipated by either one of Mitani (USPN 6,663,986) or Fujimoto et al. (USPN 6,377,500). Bruce et al., Mitani, and Fujimoto et al. together are referred to hereinafter collectively as the "cited references".

Discussion of Rejection

Prima facie case of non-patentability not met

It is Applicants' position that the reasoning set forth in the Office action for rejecting claims 1-44 are so minimal and unspecific with respect to the claims and the cited references that the Office has failed meet its burden of

presenting at least a prima facie case of non-patentability. More particularly, the Office has failed to meet its burden of proving anticipation.

As stated by the Court of Appeals for the Federal Circuit, "Under section 102(b), anticipation requires that the prior art reference disclose, either expressly or under the principles of inherency, every limitation of the claim. . . .The examiner bears the burden of presenting at least a prima facie case of anticipation. Only if that burden is met, does the burden of going forward shift to the applicant." *In re Sun*, 31 U.S.P.Q.2D (BNA) 1451 (Fed. Cir. 1993)(citations omitted)(emphasis added).

As stated by the Board of Patent Appeals and Interferences, "It is incumbent upon the examiner to identify wherein each and every facet of the claimed invention is disclosed in the applied reference. *Ex parte Levy*, 17 USPQ2d 1461, 1462 (Bd. Pat. App. & Int'f 1990)(emphasis added).

Finally, as noted in § 707.06 of the Manual of Patent Examining Procedure (MPEP): "The pertinence of each reference, if not apparent, must be clearly explained and each rejected claim specified." (emphasis added).

In rejecting the pending claims of the present application the Office stated:

> Claims 1 – 44 are rejected under 35 USC 102 (b) as being clearly anticipated by Bruce et al., U.S. 6,000,006.
>
> *As presently written, the claims are quite broad, to the extent that they would have been taught by a system that utilized a*

random access memory to store logical-to-physical address mapping information for an associated flash memory, with all the usual procedures utilized with such a map when modification or erasure has occurred. Bruce et al. taught such a system. Note Figures 4 and 6 and column 6.

Claims 1 – 44 are rejected under 35 USC 102 (b) as being clearly anticipated by either one of Mitani (USPN 6,663,986) or Fujimoto et al. (USPN 6,377,500).

As presently written, the claims are quite broad, to the extent that they would have been taught by a system that utilized a random access memory to store logical-to-physical address mapping information for an associated flash memory, with all the usual procedures utilized with such a map when modification or erasure has occurred.

Mitani taught such a system. Note Figure 1.

Fujimoto et al. taught such a system. Note Figures 1, 3 and 4A.

The above quoted two paragraphs set forth the sum total of the reasoning presented by the Office for rejecting claims 1 - 44. It should be noted that the italicized portions of the two quoted two paragraphs are identical.

It is Applicants' position that the reason for rejection of the claims set forth by the Office does not rise to the level of evidence that is required for a showing of anticipation. No individual claims are called out and discussed in

the rejection. Not a single step or element of any of the claims is called out and discussed. Additionally, no particular element or step of any of the references is called out and discussed, with respect to a particular element of a claim or otherwise. With respect to the cited references, the Office merely directs the Applicants generally to a single column and two figures in Bruce et al., one figure in Mitani, and 3 figures in Fujimoto et al.

The reasons present by the Office for rejecting claims 1-44 are so minimal and unspecific that to fully respond, the Applicants would be required to go through each reference in detail and guess at which elements and steps the Office believes correspond to the elements of the claims. Put another way, the Applicants have been given the burden of using the cited references to attempt to make out a case of anticipation against each of their own claims, and then to rebut that case. Placing such a burden of the Applicants is clearly contrary to well establish PTO practice and the law.

It is, therefore, Applicants' position that the Office has failed to meet its burden of establishing a prima facie case of nonpatentability with respect to any of claims 1 – 44.

Claims rejected improperly expressed

As noted in § 707.07 of the Manual of Patent Examining Procedure (MPEP), "A plurality of claims should never be grouped together in a common

rejection, unless that rejection is equally applicable to all claims in the group." (emphasis added).

Each of claims 1 - 44 were rejected in a single rejection, as set forth above. As such, it is Applicants' position that the bulk rejection of claims 1 – 44 is an improper omnibus rejection.

With the above discussion in mind, the Applicants respectfully request that in all future Office actions relating to the present application, the Office specifically address each element of a claim individually, or at least specifically address similar claim elements from various claims as a group. Additionally, Applicants respectfully request that the Office indicate with reasonable specificity where elements of any rejected claim are believed to be shown in an applied reference.

Discussion of Claim Rejections

Claim 1 reads as follows:

1. A method comprising:

receiving a request to write data to a logical sector address of a flash memory medium;

selecting a physical sector address from a list of free physical sector addresses;

assigning the selected free physical sector address to the logical sector address forming a corresponding relationship between the addresses;

storing the corresponding relationship between the addresses in a data structure; and

writing the data into a physical sector of the flash memory medium at a location indicated by the selected free physical sector address.

Claim 1 recites selecting a free physical sector address from a list of free physical sector addresses and writing data to a physical address indicated by the selected free physical sector address. As noted on page 13, lines 11-12 of the present application, "a free physical sector is any sector that can accept data without the need to be erased first."

Applicants have reviewed each of the cited references in detail and could find nothing in any of the cited references that teaches or suggests the concept of a list of free physical sector addresses, of selecting a physical sector address from a list of free physical sectors, or writing data into a physical sector at a location indicated by the selected free physical sector address, as recited in claim 1.

Claim 1 recites assigning the selected free physical sector address to the logical sector address forming a corresponding relationship between the addresses, and storing the corresponding relationship between the addresses in a data structure. As noted above, the cited references do not teach logical-to-physical **sector** mapping. The concept of associating logical and physical **sector** addresses and storing this association in a data structure is simply not described in the cited

references. As such, the cited references do not teach either the "forming" or "storing" operations of claim 1.

As described, the cited references fail to teach or suggest all of the steps recited in claim 1. As such, it is believed that claim 1 is allowable over the cited references, and such allowance is respectfully requested.

Claims 2-6 each depend in some form from claim 1 and, therefore, necessarily include all of the steps recited in claim 1. As such, each of claims 2-6 is allowable over the cited references for at least the reasons set forth with respect to claim 1. Each of claims 2-6 also specifies an additional feature or features that, together with the steps of claim 1, define a unique method that is not taught or suggested by the cited references.

Claims 7 – 14 have been canceled.

Claim 15 reads as follows:

15. A computer-readable medium having computer-executable instructions for performing steps comprising:

receiving a request to write data to a logical sector address of a flash memory medium;

selecting a physical sector of the flash memory medium to store the data based on the ability of the physical sector to store the data without first being erased;

assigning a physical sector address of the selected physical sector to the logical sector address forming a corresponding relationship between the addresses;

storing the corresponding relationship between the addresses in a data structure;

writing the data into the physical sector; and

writing the logical sector address in the physical sector of the flash memory medium along with the data.

Claim 15 recites, receiving a request to write data to a logical sector address and selecting a physical sector to store the data based on the ability of the physical sector to store the data without first being erased. Applicants have reviewed each of the cited references in detail and could find nothing in any of the cited references that teaches selecting a physical sector to store the data based on the ability of the physical sector to store the data without first being erased.

Claim 15 recites assigning a physical sector address to the logical sector address forming a corresponding relationship between the addresses, and storing the corresponding relationship between the addresses in a data structure. As noted above, the concept of associating logical and physical sector addresses and storing this association in a data structure is simply not described in the cited references.

As such, the cited references do not teach either the "forming" or "storing" operations of claim 15.

Claim 15 also recites writing the logical sector address in the physical sector of the flash memory medium along with the data. Applicants could find nothing in any of the cited references that teaches writing a logical sector address in a physical sector of the flash memory medium along with the data.

As described, the cited references fail to teach the combination of steps recited in claim 15. As such, claim 15 is believed to be allowable over the cited references, and such allowance is respectfully requested.

Claims 16 – 20 each depend in some form from claim 15 and, therefore, each of these claims includes all of the steps recited in claim 15. Each of claims 16 – 20 is believed to be allowable over the cited references for at least the reasons set forth with respect to claim 15. Each of claims 16 – 20 also includes a step or steps in addition to the steps of claim 15. As such, each of claims 16 – 20 recites a unique combination of steps that is believed to be allowable over the cited references.

Claim 21 has been canceled.

Claim 22 reads as follows:

22. A method comprising:

(a) receiving a request to write data to a logical sector address of a flash memory medium;

(b) assigning a physical sector address to the logical sector address forming a corresponding relationship between the addresses;

(c) storing the corresponding relationship between the addresses in a data structure;

(d) writing the data into a physical sector of the flash memory medium at a location indicated by the physical sector address;

(e) receiving a request to rewrite updated data to the logical sector address;

(f) assigning a new physical sector address to the logical sector address forming a corresponding relationship between the new physical sector address and the logical sector address;

(g) storing the corresponding relationship between the addresses from the aforementioned paragraph (f) in the data structure;

(h) writing the updated data into a physical sector of the flash memory medium at a location indicated by the new physical sector address; and

(i) marking the physical sector address from the aforementioned paragraph (b) as dirty.

Claim 22 relates to, among other things, satisfying a request to write updated data to a given logical sector address by writing the updated data to a new physical sector and assigning the physical sector address of the new physical sector to the given logical sector address.

Applicants have been unable to locate any discussion in any of the cited references related to the general concept of handling the rewriting of updated data to a logical sector address in a flash device, much less handling the rewriting of updated data in the manner recited in claim 22. With this in mind, steps (e) – (f) are clearly not taught in any of the cited references.

Claim 22 recites assigning a physical sector address to the logical sector address forming a corresponding relationship between the addresses, and storing the corresponding relationship between the addresses in a data structure. As noted above, the concept of associating logical and physical sector addresses and storing this association in a data structure is simply not described in the cited references. As such, the cited references do not teach either the "forming" or "storing" operations of claim 22.

Claim 22 recites marking the physical sector address from the aforementioned paragraph (b) as dirty. As noted in the present application in the last paragraph of page 14, a dirty sector is a sector that has had its data written to another physical sector. Applicants have been unable to locate any discussion in any of the cited references related to marking a physical sector address as dirty.

As described, the cited references fail to teach or suggest the combination of steps recited in claim 22. As such, claim 22 is believed to be allowable over the cited references, and such allowance is respectfully requested.

Claims 23 – 26 each depend in some form from claim 22. As such, each of claims 23-26 is necessarily allowable over the cited references for at least the reasons set forth with respect to claim 22. Each of claims 23 – 26 also includes a step or steps in addition to the steps of claim 22. As such, each of claims 23 – 26 recites a unique combination of steps that is believed to be allowable over the cited references.

Claim 27 has been canceled.

Claim 28 reads as follows:

28. A system, comprising:

flash medium logic, configured to store data in a physical sector of a flash memory medium;

a table, configured to map logical sector addresses received from a file system to physical sector addresses on the flash memory medium; and

flash abstraction logic, configured to ascertain a next free physical sector on a flash memory medium and assign an address associated with the free physical sector to a logical sector address associated with a write request received from the file system.

Claim 28 recites a table that is configured to map logical sector addresses received from a file system to physical sector addresses on the flash memory medium. As previously mentioned, none of the cited references describe the use of logical-to-physical **sector** mapping.

Claim 28 also recited a flash abstraction logic that is configured to ascertain a next free physical sector on a flash memory medium and assign an address associated with the free physical sector to a logical sector address associated with a write request received from the file system. Applicants have reviewed each of the cited references in detail and could find nothing in any of the cited references that teaches ascertaining a next free physical sector to store the data based on the ability of the physical sector to store the data without first being erased.

As described, the cited references fail to teach or suggest the combination of elements recited in claim 28. As such, claim 28 is believed to be allowable over the cited references, and such allowance is respectfully requested.

Claims 29 – 35 each depend in some form from claim 28. As such, each of claims 29 - 35 is necessarily allowable over the cited references for at least the reasons set forth with respect to claim 28. Each of claims 29 - 35 also recite various features in addition to the elements of claim 28. As such, each of claims 29 - 35 recites a unique combination of elements that is believed to be allowable over the cited references.

Claim 36 reads as follows:

36. A computer-readable medium for a flash driver, comprising computer-executable instructions that, when executed, direct the flash driver to:

receive a request to write data to a logical sector address of a flash memory medium;

selecting a physical sector address from a list of free physical sector addresses;

assign [[a]] the selected physical sector address to the logical sector address forming a corresponding relationship between the addresses;

store the corresponding relationship between the addresses in a table; and

write the data into a physical sector of the flash memory medium at a location indicated by the physical sector address.

Claim 36 recites selecting a free physical sector address from a list of free physical sector addresses and writing data to a physical address indicated by the selected free physical sector address. As noted above with respect to claims 1, Applicants have reviewed each of the cited references in detail and could find nothing in any of the cited references that teaches or suggests the concept of a list of free physical sector addresses, of selecting a physical sector address from a list of free physical sectors, or writing data into a physical sector at a location indicated by the selected free physical sector address, as recited in claim 36.

Claim 36 also recites assigning a physical sector address to the logical sector address forming a corresponding relationship between the addresses, and storing the corresponding relationship between the addresses in a data structure. As noted above, the concept of associating logical and physical sector addresses and storing this association in a data structure is simply not described in the cited references. As such, the cited references do not teach either the "forming" or "storing" operations of claim 36.

As described, the cited references fail to teach or suggest all of the steps recited in claim 36. As such, it is believed that claim 36 is allowable over the cited references, and such allowance is respectfully requested.

Claim 37 reads as follows:

37. A computer-readable medium for a flash driver, comprising computer-executable instructions that, when executed, direct the flash driver to:

receive a request to write data to a logical sector address of a flash memory medium;

assign a physical sector address to the logical sector address forming a corresponding relationship between the addresses;

store the corresponding relationship between the addresses in a table;

write the data into a physical sector of the flash memory medium at a location indicated by the physical sector address;

write the logical sector address in the physical sector of the flash memory medium along with the data;

if the table is erased, then scan the flash memory medium to locate the logical sector address stored with the data;

assign the physical sector address containing the data to the logical sector address forming a reestablished corresponding relationship between the addresses; and

store the reestablished corresponding relationship between the addresses in a new table.

Claim 37 recites a computer-readable medium comprising computer-executable instructions that assign a physical sector address to a logical sector address forming a corresponding relationship between the addresses, and store the corresponding relationship between the addresses in a table. As noted above, the concept of associating logical and physical sector addresses and storing this association in a data structure is simply not described in the cited references. As such, the cited references do not teach either the "form" or "store" element of claim 37.

The computer executable instructions of claim 37 also write the logical sector address in the physical sector of the flash memory medium along with the data. Applicants could find nothing in any of the cited references that teaches

writing a logical sector address in a physical sector of the flash memory medium along with the data.

The computer executable instructions of claim 37 also scan the flash memory medium to locate the logical sector address stored with the data if the table is erased, assign the physical sector address containing the data to the logical sector address forming a reestablished corresponding relationship between the addresses, and store the reestablished corresponding relationship between the addresses in a new table.

It follows, that since the cited references do not teach storing the correspondence between logical and physical addresses in a table, or writing a logical sector address in a physical sector of the flash memory medium along with the data, the cited references likewise do not show reestablishing a new table if old table is erased, as recited in the last three elements of claim 37.

As described, the cited references fail to teach or suggest all of the steps recited in claim 37. As such, it is believed that claim 37 is allowable over the cited references, and such allowance is respectfully requested.

Claim 38 reads as follows:

38. A system for tracking sectors in a flash memory medium, comprising:

means for receiving a request to retrieve data stored in the flash memory medium from a location indicated by a logical sector address;

means for locating a physical sector address corresponding to the specific logical sector address in a table; and

means for reading the data stored in the flash memory medium from the physical sector address located from the table.

Claim 38 recites means for locating a physical sector address corresponding to the specific logical sector address in a table. As previously mentioned, none of the cited references describe the use of logical-to-physical **sector** mapping. More particularly, the cited references do not show locating a physical **sector** address corresponding to the specific logical **sector** address in a table.

As described, the cited references fail to teach or suggest all of the steps recited in claim 38. As such, it is believed that claim 38 is allowable over the cited references, and such allowance is respectfully requested.

Claims 39 – 44 each depend in some form from claim 38. As such, each of claims 39 - 44 is necessarily allowable over the cited references for at least the reasons set forth with respect to claim 38. Each of claims 39 - 44 also recite various features in addition to the elements of claim 38. As such, each of claims 39 - 44 recites a unique combination of elements that is believed to be allowable over the cited references.

Conclusion

Claims 1 – 6, 15 – 20, 22 – 26, and 28 - 44 are believed to be in condition for allowance. Applicant respectfully requests reconsideration and prompt issuance of the present application. Should any issue remain that prevents immediate issuance of the application, the Office is encouraged to contact the undersigned attorney to discuss the unresolved issue.

Respectfully Submitted,

Dated: 5-19-04

By: _____

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